AMENDMENTS TO THE SPECIFICATION:

IN THE SPECIFICATION:

Please replace the paragraph beginning at page 24, line 17 with the following:

A non-volatile memory cell (simply referred to as a memory cell) MC illustrated in FIG. 3 is constituted to have an MOS type memory transistor portion 26 to be used for storing information and an MOS type selecting transistor portion 27 for selecting the memory transistor portion 26 in a p-type well region 25 provided on a silicon substrate. The memory transistor portion 26 has an n-type diffusion layer (an n-type impurity region) 30 to be a source line connecting electrode to be connected to a source line, an electric charge storage insulating film (for example, a silicon nitride film) 31, insulating films (for example, silicon oxide films) 32 and 33 provided on the upper and lower sides of the electric charge storage insulating film 31, and a memory gate electrode (for example, an n-type polysilicon layer) 34 for applying a high voltage in a write processing and an erase processing. For example, the insulating film 32 is set to have a thickness of 5 nm, the electric charge storage insulating film 31 is set to have a thickness of 10 nm (a silicon oxide film conversion), and the insulating film 33 is set to have a thickness of 3 nm.

The selecting transistor portion 27 has an n-type diffusion layer (an n-type impurity region) 35 to be a bit line connecting electrode to be connected to a bit line, a gate insulating film (for example, a silicon oxide film) 36, a control gate electrode (for example, an n-type polysilicon layer) 37, and an insulating film (for example, a silicon oxide film) 38 for insulating the control gate electrode 37 from the memory gate electrode ~~14~~34.